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## IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of:			
	Kun-Yung K. Chang and Jason C. Wei	)	
Application No. 09/941,079			
Filed:	August 28, 2001	)	
For:	CLOCK DATA RECOVERY WITH SELECTABLE PHASE CONTROL INPUT	) ) _)	

Assistant Commissioner for Patents Washington, D.C. 20231

Examiner: Not Yet Assigned

Art Unit: Not Yet Assigned

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**PATENT** 

Charles E. Shemwell

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By:

Respectfully submitted,

Date: Sept. 25, 2001

Charles E. Shemwell, Reg. No. 40,171

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet of 1 1

Complete if Known					
Application Number	09/941,079				
Filing Date	August 28, 2001				
First Named Inventor	Kun-Yung K. Chang				
Group Art Unit					
Examiner Name					
Attorney Docket Number	R1-P101				

	OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS					
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"Cypre	ess Applications Handbook," Cypress Semiconductor Corporation, 1996, pp. 6-26 to 6-33					
"An Integratable 1-2.5 Gbps Low Jitter CMOS Transceiver with Built in Self Test Capability," Ah-Lyan Yee, Richard Gu, et al., Symposium on VLSI Circuits Digest of Technical Papers, 1999, pp. 45-46						
"A Ser Journa	"A Semidigital Dual Delay-Locked Loop," Stefanos Sidiropolous and Mark A. Horowitz, IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp.1683-1692					
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<sup>&</sup>lt;sup>1</sup> Unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.